## Inside the Machine

## An Illustrated Introduction to Microprocessors and Computer Architecture

by Jon Stokes
errata updated to print 6

| Page | Error |  |  |  | Correction |  |  |  | $\begin{gathered} \text { Print } \\ \text { corrected } \end{gathered}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | All of them rely on a limited repertoire of technologies that enable them do the myriad kinds of miracles we've come to expect from them. |  |  |  | All of them rely on a limited repertoire of technologies that enable them to do the myriad kinds of miracles we've come to expect from them. |  |  |  | Print 3 |
| 93 |  | Pentium Pro Vitals | Pentium II <br> Vitals | Pentium III Vitals |  | Pentium Pro Vitals | Pentium II <br> Vitals | Pentium III Vitals | Print 2 |
|  | Introduction <br> Date | $\begin{aligned} & \text { November 1, } \\ & 1995 \end{aligned}$ | May 7, 1997 | $\begin{aligned} & \text { February 26, } \\ & 1999 \end{aligned}$ | Introduction <br> Date | $\begin{array}{\|l} \text { November 1, } \\ 1995 \end{array}$ | May 7, 1997 | $\begin{aligned} & \text { February 26, } \\ & 1999 \end{aligned}$ |  |
|  | Process | $\begin{aligned} & 0.60 / 0.35 \\ & \text { micron } \end{aligned}$ | 0.35 micron | 0.25 micron | Process | $\begin{aligned} & 0.60 / 0.35 \\ & \text { micron } \end{aligned}$ | 0.35 micron | 0.25 micron |  |
|  | Transistor Count | 5.5 million | 7.5 million | 9.5 million | Transistor Count | 5.5 million | 7.5 million | 9.5 million |  |
|  | Clock Speed at <br> Introduction | $\begin{aligned} & 150,166,180, \\ & \text { and } 200 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 233,266, \text { and } \\ & 300 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 450 \text { and } 500 \\ & \mathrm{MHz} \end{aligned}$ | Clock Speed at <br> Introduction | $150,166,180,$ $\text { and } 200 \mathrm{MHz}$ | $\begin{aligned} & 233,266, \text { and } \\ & 300 \mathrm{MHz} \end{aligned}$ | $\begin{aligned} & 450 \text { and } 500 \\ & \mathrm{MHz} \end{aligned}$ |  |
|  | L1 Cache Size | 8KB instruction, 8KB data | 16 KB instruction, 16 KB data | 16 KB instruction, 16 KB data | L1 Cache Size | 8KB <br> instruction, 8KB data | 16KB instruction, 16 KB data | 16 KB instruction, 16 KB data |  |
|  | L2 Cache Size | 256 KB or 512KB (ondie) | 512KB (offdie) | $\begin{aligned} & \text { 512KB (on- } \\ & \text { die) } \end{aligned}$ | L2 Cache Size | $\begin{array}{\|l} 512 \mathrm{~K} \text { or } 1 \mathrm{MB} \\ \text { (off-die) } \end{array}$ | $512 \mathrm{~KB} \text { (off- }$ die) | $\begin{aligned} & 256 \mathrm{~K} \text { or } 512 \mathrm{~K} \\ & \text { (on-die) } \end{aligned}$ |  |
|  | x86 ISA <br> Extensions |  | MMX | SSE added in 1999 | x86 ISA <br> Extensions |  | MMX | SSE added in 1999 |  |

